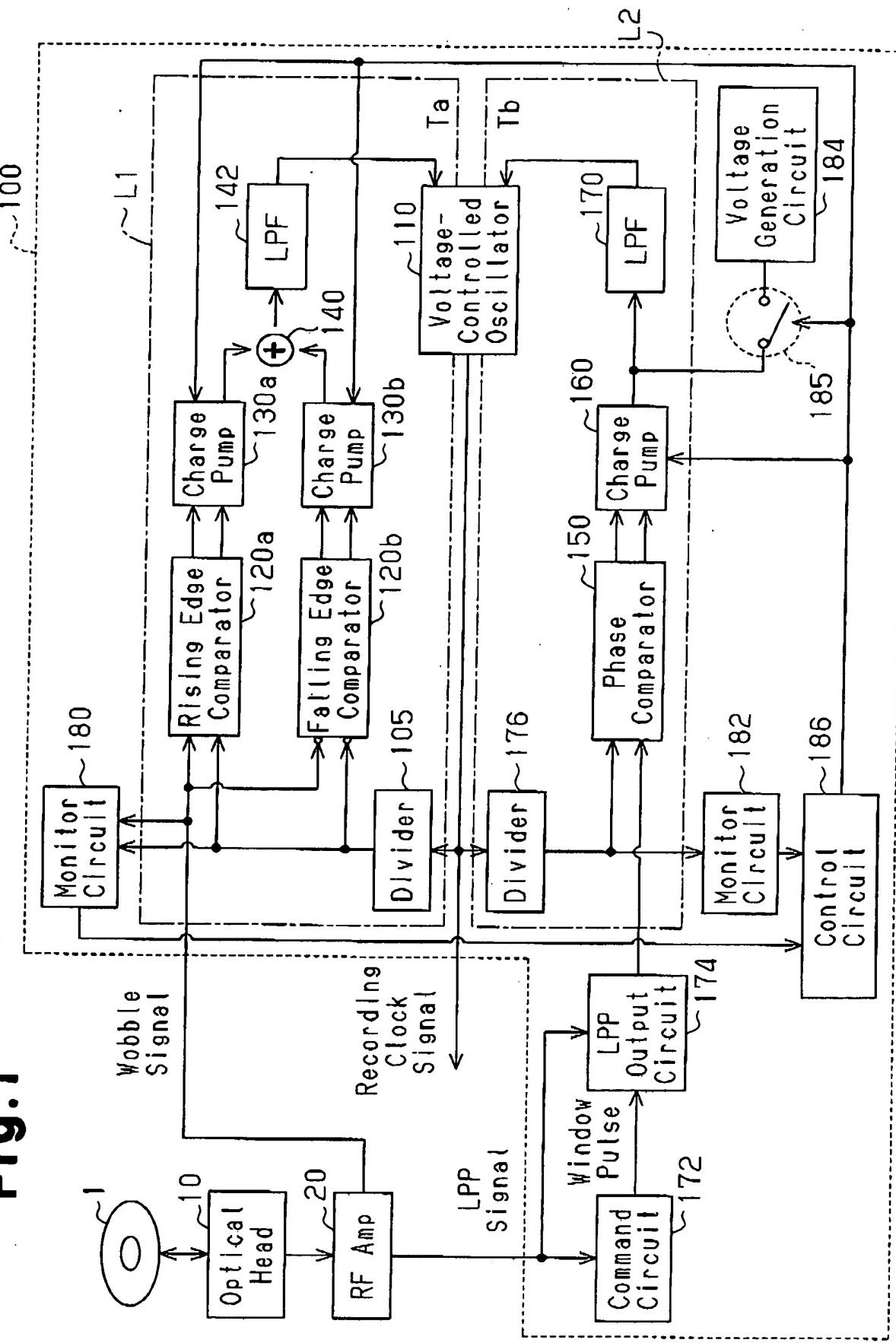
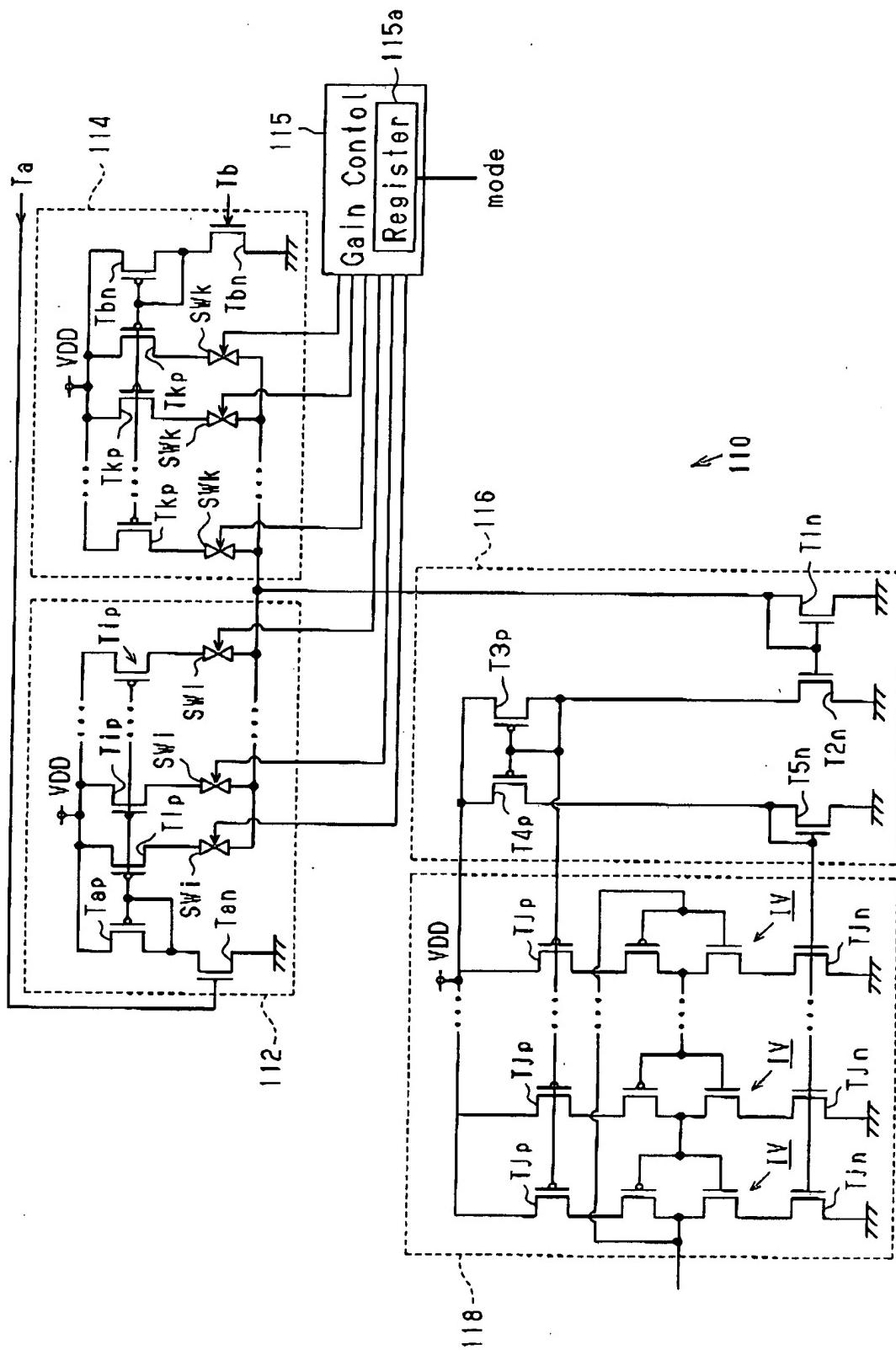


Fig. 1

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 PHASE LOCKED LOOP CIRCUIT

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Fig. 2

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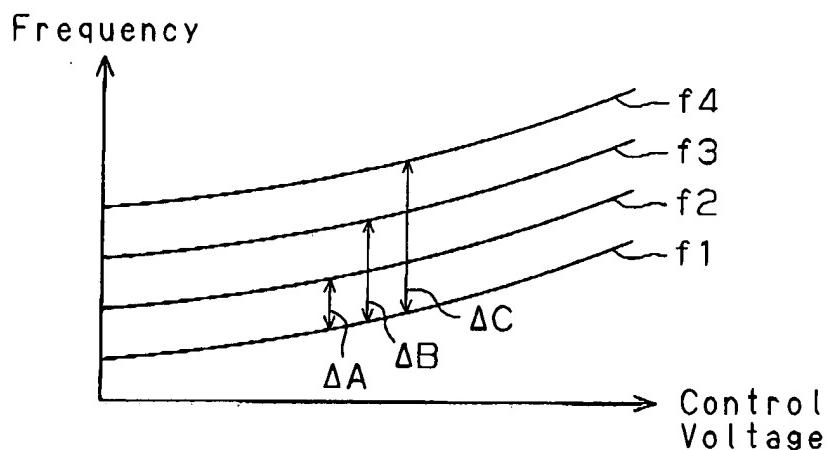
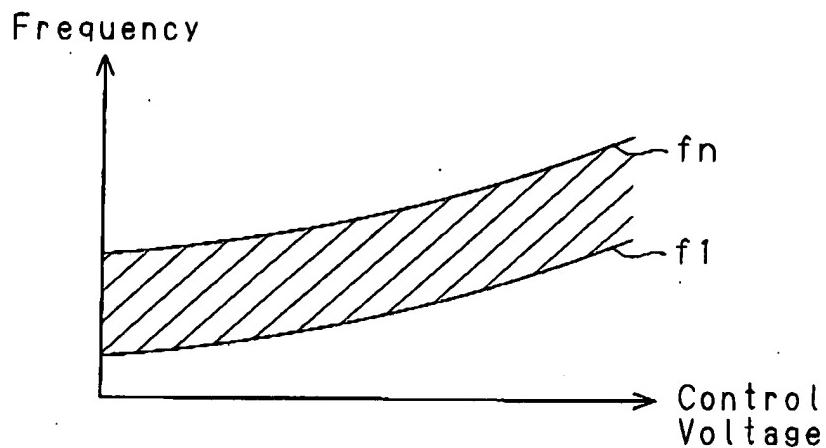
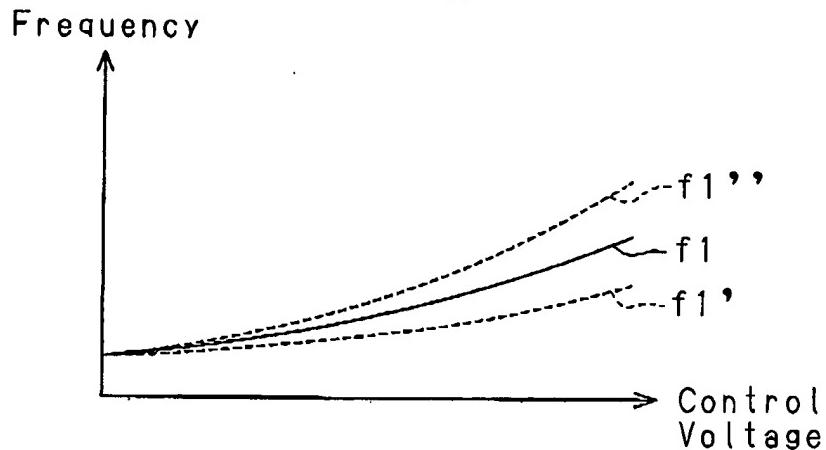
Fig.3**Fig.4****Fig.5**

Fig. 6A Fig. 6B

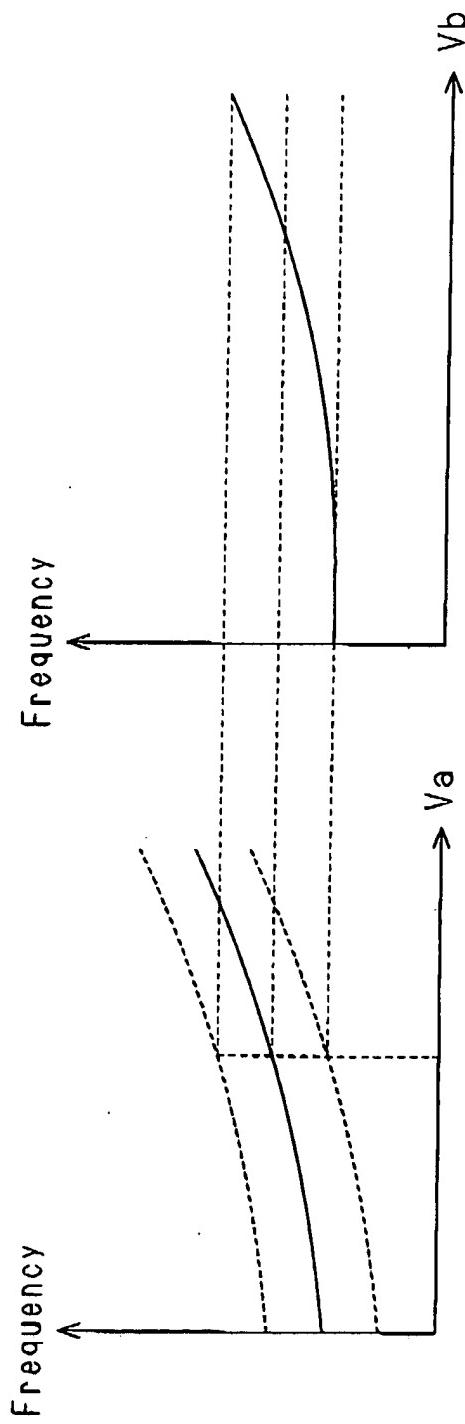


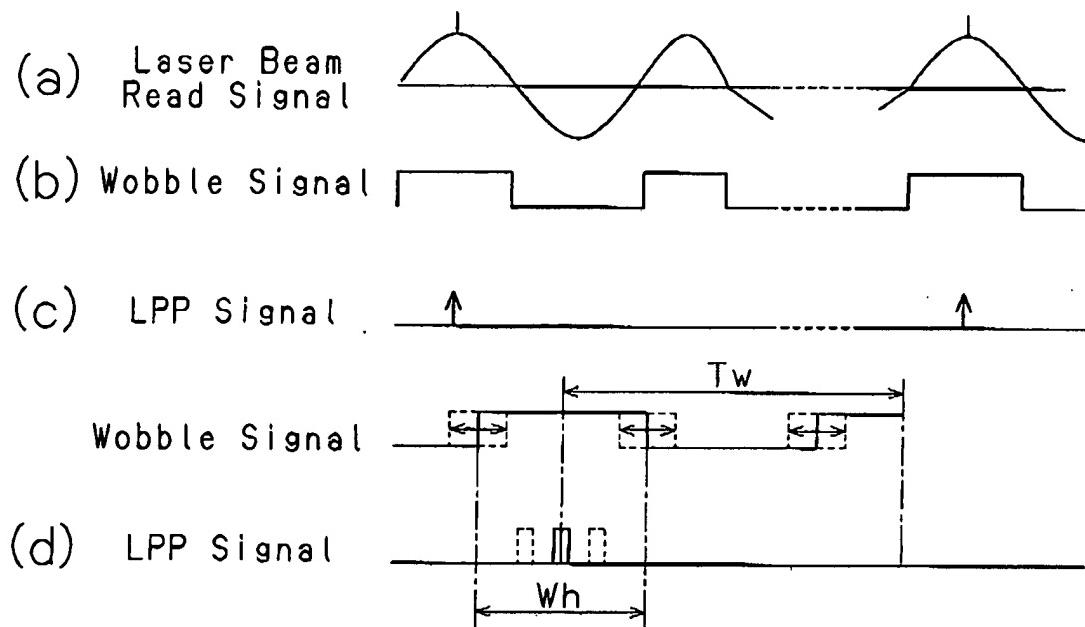
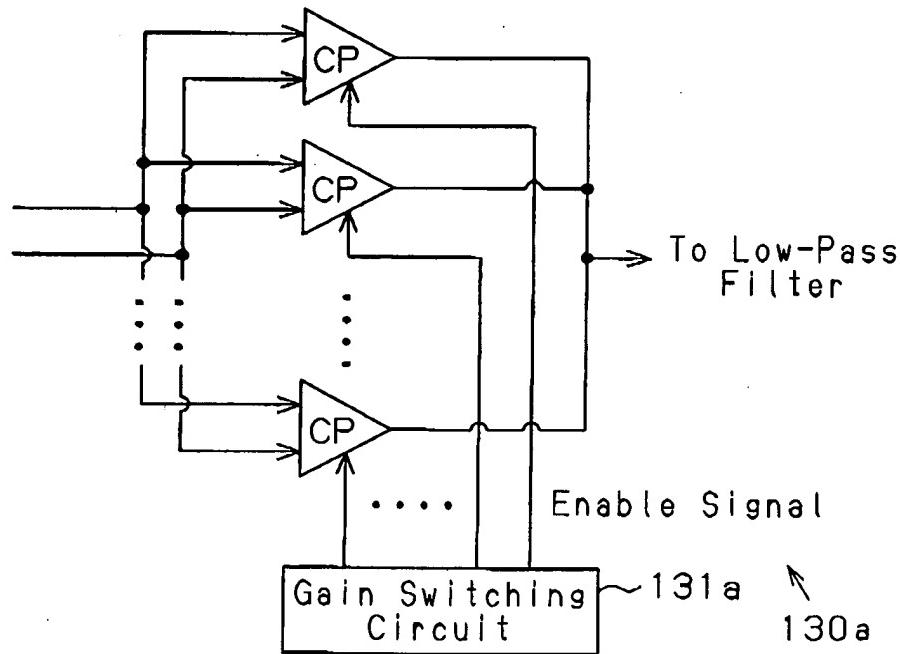
Fig.7**Fig.8**

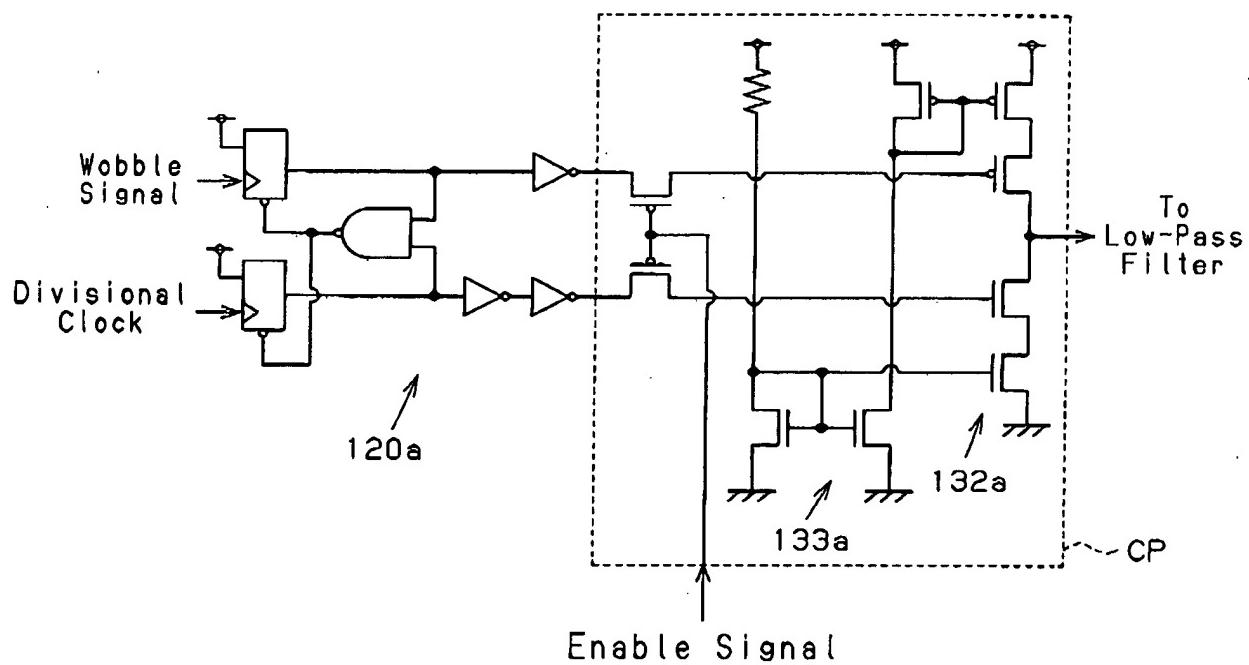
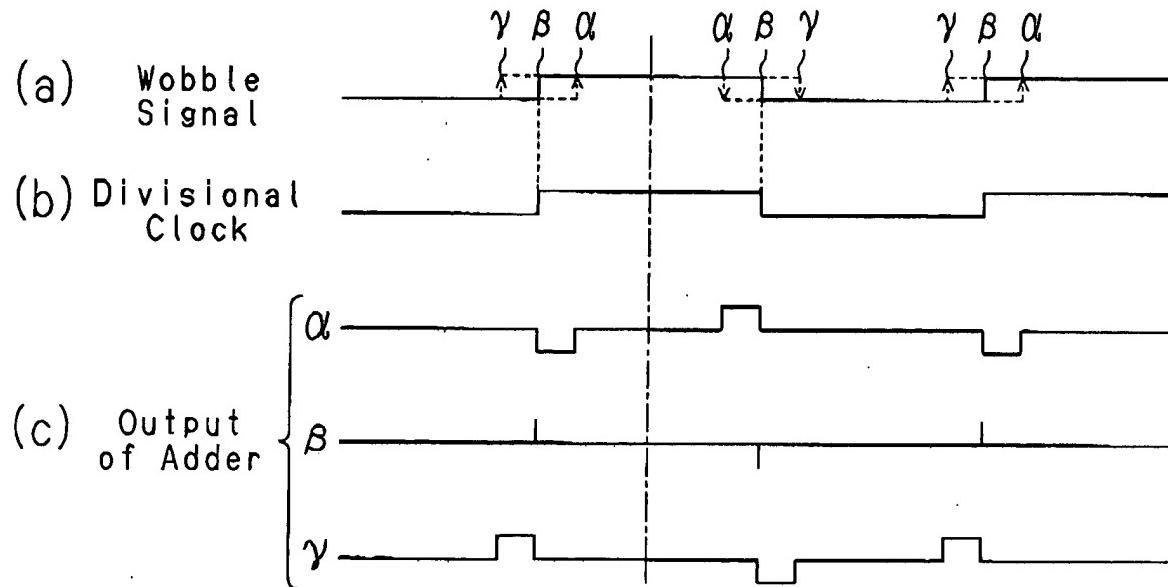
Fig.9**Fig.10**

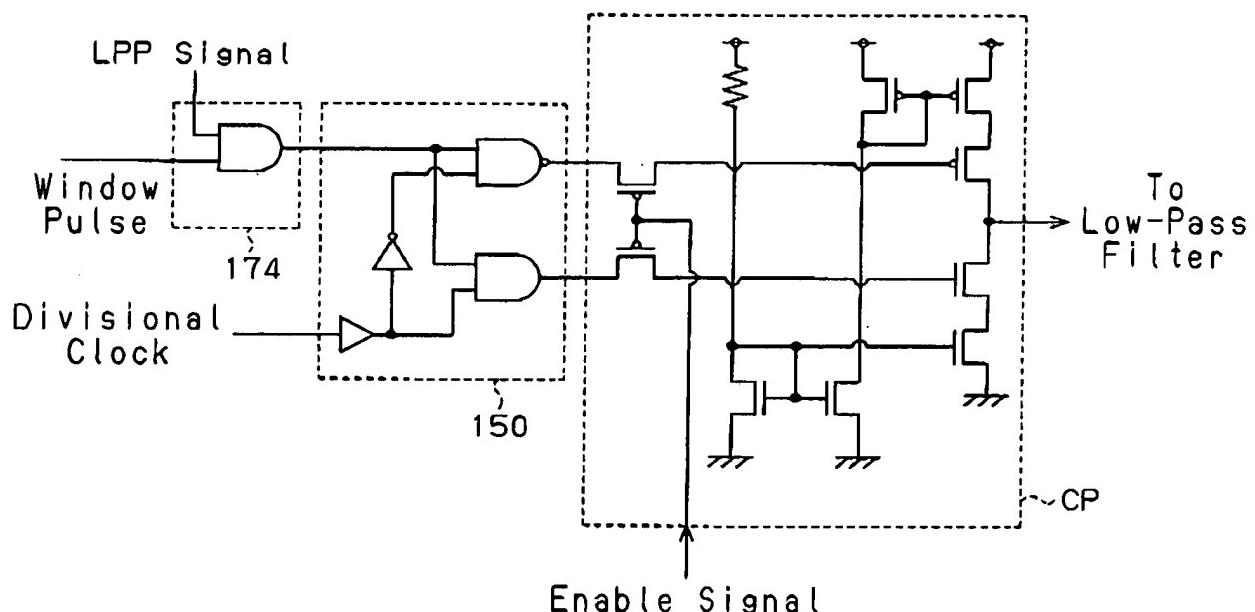
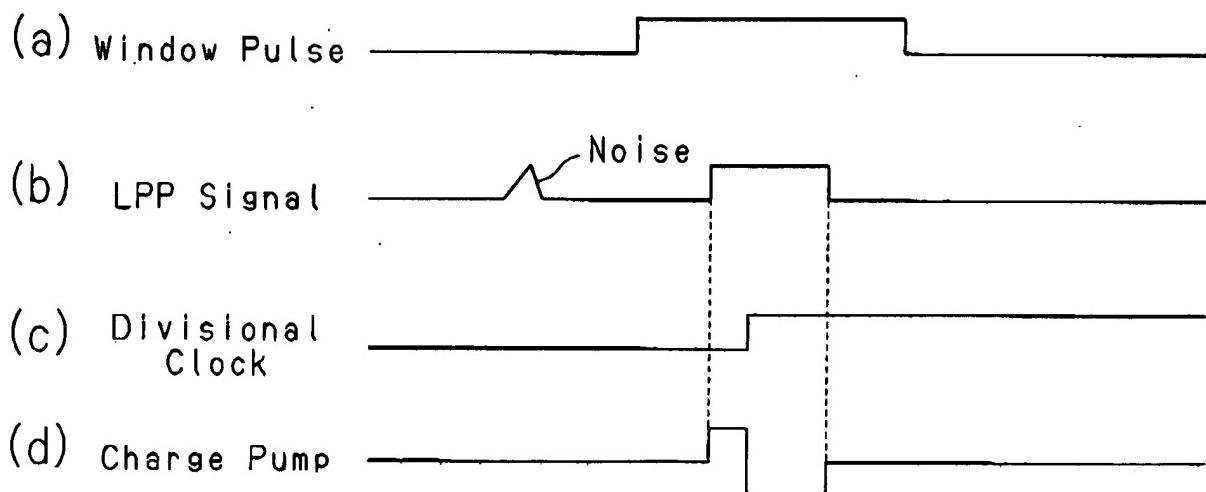
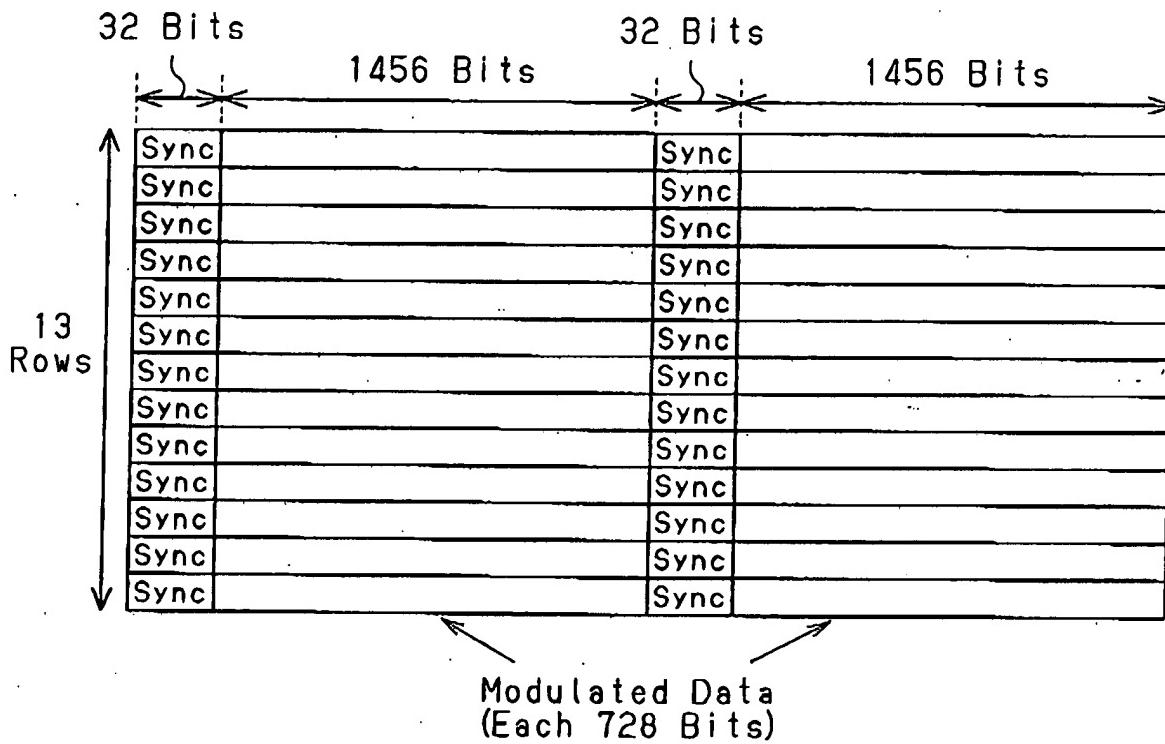
Fig.11**Fig.12**

Fig.13**Fig.14**